VERSATILE SYSTEM FOR INTEGRATED SENSE TRANSISTOR

TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to semiconductor circuitry and, more particularly, to a system for providing highly accurate sense transistor circuitry.

BACKGROUND OF THE INVENTION

In a number of modern electronics systems, various transistor structures are designed to operate at, and withstand, different voltage and current levels. For example, numerous designs commonly utilize high-voltage "power" transistors in conjunction with low-voltage transistors. Generally, most designs seek to minimize the number of "power" transistors—as such components are relatively expensive and cumbersome, when compared to their low-voltage counterparts. To this end, and in order to successfully interface higher voltage transistors to their low-voltage counterparts, many designs pair high power transistor structures with some configuration of lower power sensing transistors.

Commonly, sensing transistors are configured in a manner that divides or scales down voltage or current levels across the high power transistor, such that those levels can be measured and processed with low-power, cost-efficient transistors. A voltage or current parameter across one low-power sensing transistor may then be measured or processed, as representative of a pre-determined fraction of that same parameter across the power transistor.

In the past, the level of accuracy with which such sensing approximations were made was—in some cases—marginal. At the time, however, system using such approaches may not have needed highly accurate sensing. As the demands on signal communications and processing systems have steadily increased, though, the need for greater accuracy and precision in sensing transistor arrangements has also increased.

Most conventional sensing transistor arrangements commonly involve a power transistor fabricated on the same die as one or more sensing transistors. For example, a CMOS power FET may have one or more sense FETs fabricated on the same die. In some instances, a sense FET may be physically located some distance on the die from the power FET, or it may be located directly about the perimeter thereof.

Conventionally, addressing the accuracy of sense FETs concerns matching—as closely as possible—the fabrication characteristics of a sense FET to a power FET. Even where a sense FET is fabricated around the immediate perimeter of a power FET, only a limited level of matching or accuracy can be attained. Fabrication and processing variations between the transistor structures in the center of a large power FET and a sense FET around the outer perimeter of the power FET commonly result in some nominal degree of mismatch—thereby limiting the achievable accuracy level of conventional sense FET designs. Thermal variations between the area of the sense FET and the area of the power FET can also further contribute to mismatch.

In addition to the physical considerations, there are also now a number of parametric considerations that may impact the usefulness of conventional sense transistor configurations. For example, there are a number of advanced power transistor designs that—to a certain extent—render such conventional sense transistor topologies inefficient or infeasible. These power transistor designs may be optimized for operational parameters—such as extremely low on resistance (R_{on})—that make conventional divide or scale down sensing impractical.

As a result, there is a need for a system that provides highly accurate sense transistor circuitry—one that optimizes matching of sense and power transistor structures, and minimizes or obviates thermal and fabrication variations—in a versatile, cost-effective, commercially-viable manner.

SUMMARY OF THE INVENTION

The present invention provides a versatile system, comprising various constructs and methods, for providing a sense transistor structure—particularly a sense FET—optimally matched with an associated power transistor. The system of the present invention integrates one or more sense transistor structures within the architecture of a power transistor. The sense transistor architecture of the present invention shares architectural and parametric characteristics with the power transistor—optimizing lithographic matching and thermal coupling, and obviating the need for divide-down architectures. The system of the present invention thus compensates for, and overcomes, fabrication or processing variations across a given area—and is easily implemented within a number of commercially viable semiconductor layout and process technologies.

Specifically, the present invention provides an architecture that produces sense transistors having optimized thermal and parametric matching with an associated power transistor. A power transistor is formed, having a plurality of alternating source and drain structures, with a plurality of gate structures interposed there between. At a desired location within the power transistor—which may be in a central location, or symmetrically distributed—one or more sense transistors are formed from an isolated portion of either a drain or source structure. The sense transistor structure may then be utilized in conjunction with a variety of current or voltage measurement circuitry.

Other features and advantages of the present invention will be apparent to those of ordinary skill in the art upon reference to the following detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the invention, and to show by way of example how the same may be carried into effect, reference is now made to the detailed description of the invention along with the accompanying figures in which corresponding numerals in the different figures refer to corresponding parts and in which:

FIGS. **1***a*, **1***b*, and **1***c* provide illustrations depicting one embodiment of a transistor architecture illustrating certain aspects of the present invention;

FIG. **2** provides an illustration depicting another embodiment of a transistor architecture illustrating certain aspects of the present invention; and

FIG. **3** provides an illustration depicting one embodiment of a transistor structure according to certain aspects of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

While the making and using of various embodiments of the present invention are discussed in detail below, it should be appreciated that the present invention provides many applicable inventive concepts, which can be embodied in a wide